IN THE CLAIMS

Please amend the claims as follows:

1.- 47. (Canceled)

48.(Previously Presented) A contact hole for a semiconductor device, comprising:

a bottom surface of a first material;

at least one vertical sidewall of a second material;

a generally planar layer of a third material covering only the bottom surface, the third material having a graded stoichiometry between a refractory metal and the first material.

49.(Original) The contact hole of claim 48 where the hole has a high aspect ratio.

50. (Original) The contact hole of claim 48 where the first material is silicon.

51. (Original) The contact hole of claim 48 where the second material is an insulator.

52. (Original) The contact hole of claim 48 where the planar layer contacts the sidewalls.

53. (Original) The contact hole of claim 52 where the third material is substantially confined to the bottom of the hole.

54. (Original) The contact hole of claim 48 where the third material is a silicide.

71-81 (Canceled)

82.(Original) In a semiconductor device having a substrate, a contact hole in a layer of insulator material directly overlying the substrate, the hole comprising:

a vertical sidewall consisting substantially entirely of the aforementioned layer of insulator material; and

a bottom surface having at least one generally planar bottom layer of conductive material having a graded stoichiometry between two different constituent elements in the bottom layer.

83. (Original) The device of claim 82 where the substrate is silicon and the insulator material is an oxide, a nitride, or a glass.

84. (Original) The device of claim 82 where the planar layer comprises multiple layers having mutually different stoichiometries.

85. (Original) The device of claim 82 where the conductive material includes a silicide of a metal.

86. (Original) The device of claim 85 where the metal is a refractory metal.

87.(Previously Presented) In a semiconductor device having a substrate, a contact hole in a layer of insulator material directly overlying the substrate, the hole comprising:

a bottom surface having at least one generally planar bottom layer of a conductive material including a silicide of a refractory metal, the bottom layer extending into the substrate less than twice the distance from the top of the bottom layer to the top of the substrate; and

a vertical sidewall comprising the aforementioned layer of insulator material and being free of the conductive elements.

88.(Original) The device of claim 87 where the planar layer contacts the lower end of the sidewall.

89.(Original) The device of claim 88 where the planar layer does not extend substantially up the sidewall from the bottom surface.

90.(Canceled)

91.(Previously Presented) The device of claim 87 where the planar layer is titanium silicide.

92.(Previously Presented) The device of claim 91 where the refractory metal is cobalt.

93.(Previously Presented) In a semiconductor device having a substrate, a contact hole in a layer of insulator material directly overlying the substrate, the hole comprising:

a bottom surface having at least one generally planar bottom layer of conductive material including a silicide of a metal, the silicide extending below the top of the substrate a distance less than the equilibrium ratio of the metal and the substrate material times the thickness of the bottom layer above the top of the substrate; and

a vertical sidewall comprising the aforementioned layer of insulator material, and being substantially free of the metal.

94.(Original) The device of claim 93 where the metal is a refractory metal.

95. (Original) The device of claim 93 where the insulator material is an oxide, a nitride, or a glass.

96. (Original) The device of claim 93 where the planar layer has a graded stoichiometry.

97. (Original) The device of claim 96 where the planar layer comprises multiple layers having mutually different stoichiometries.

98-104 (Canceled)

105.(Previously Presented) The integrated circuit of claim 106 where the planar layer contacts the lower end of the sidewall.

106.(Previously Presented) An integrated circuit, comprising:

a substrate;

a layer of insulating material overlying the substrate and containing at least one contact hole having only that layer as a sidewall and having a bottom surface contacting the substrate; and

at least one generally planar layer of conductive material covering the bottom surface, the planar layer including a silicide of a metal, the metal being substantially entirely confined to the bottom surface in the hole, where the planar layer has a graded stoichiometry.

107. (Previously Presented) The integrated circuit of claim 106 where the planar layer comprises multiple layers having mutually different stoichiometries.

108.(Previously Presented) A contact hole for a semiconductor device, comprising:

a bottom surface of a first material;

at least one vertical sidewall of a second material;

a generally planar layer of a silicide having a graded stoichiometry on the bottom surface.

109. (Previously Presented) The contact hole of claim 108 where the silicide includes titanium.

110. (Previously Presented) The contact hole of claim108 where the silicide includes cobalt.

111. (Previously Presented) The contact hole of claim 108 where the first material is silicon.

112. (Previously Presented) The contact hole of claim 108 where the second material is an insulator.

113. (Previously Presented) The contact hole of claim 108 where the third material is graded only on the bottom of the hole.

114.(Previously Presented) The integrated circuit of claim 106 where the contact hole has a high aspect ratio.

115.(Currently amended) In a semiconductor device, a contact hole in a layer of insulator material directly overlying the substrate, the hole comprising:

a bottom surface having at least one generally planar layer of conductive material including a silicide of a refractory metal;

a substrate having a profile that does not change significantly in the vicinity of the contact hole;

a vertical sidewall consisting substantially entirely of the aforementioned layer of insulator material; ~~The device of claim 71~~

where the profile changes less than twice the thickness of the generally planar layer.

116.(Currently amended) An integrated circuit, comprising:

a substrate;

a layer of insulating material overlying the substrate and containing at least one contact hole having only that layer as a sidewall and having a bottom surface contacting the substrate; and

at least one generally planar layer of a silicide of a refractory metal, where the profile of the substrate does not change substantially in the vicinity of the contact hole, ~~The integrated circuit of claim 98~~ where the profile changes less than twice the thickness of the generally planar layer.